ABSTRACT

A synchronous\asynchronous memory device includes a single port memory unit for storing data according to a read clock, a configurable write buffer for storing data according to a write clock and for transferring the stored data to the single port memory unit according to the read clock, a write blocking logic for controlling the configurable write buffer to store data according to a remaining data storage capability of the configurable write buffer and for controlling the configurable write buffer to transfer the stored data to the single port memory unit according to a write acknowledge signal, and an arbiter electrically connected to the write blocking logic and the single port memory unit for generating the write acknowledge signal.